

1 We claim:

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4 1) A digital gain control system comprising:

5 an rms voltage converter receiving one or more digital
6 inputs and forming an rms value;

7 a digital gain controller having:

8 an iteration variable set to an initial value;

9 a digital gain value having n bits, said digital gain
10 value having a maximum value and a minimum value, said
11 digital gain value being initially set to the median of said
12 maximum value and said minimum value;

13 a correction value having an initial value which is
14 half of said digital gain initial value;

15 an iteration process which performs the following
16 sequential steps m times:

17 comparing the value from said rms voltage converter to
18 a threshold voltage value;

19 adding said correction value if said rms voltage
20 converter is greater than said threshold voltage level, or
21 subtracting a correction value if said rms voltage converter
22 is less than said threshold voltage level;

23 halving said correction value.

24

1 2) The process of claim 1 where said m is one of the
2 values 3, 4, or 5.

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4 3) The process of claim 1 where said digital gain
5 maximum value is $2^{(n-1)}$.

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7 4) The process of claim 1 where said digital gain
8 correction value is $2^{(n-k-1)}$.

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10 5) The process of claim 1 where said digital correction
11 value is positive.

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13 6) The process of claim 1 where said digital correction
14 value is negative.

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17 7) the process of claim 1 where said iteration time has
18 a first value during a first interval, and said iteration is
19 longer than said first value during a second interval
20 following said first interval.

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22 8) The process of claim 7 where said first interval
23 corresponds to the preamble time T1 of a wireless ethernet
24 packet.

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1 9) The process of claim 7 where said second interval
2 corresponds to the frame time T2 following the preamble time
3 T1 of a wireless ethernet packet.

4
5 10) A process for generating a value Vagc where said
6 Vagc is a digital value having n bits, said process
7 comprising:

8 setting Vagc to a first value;

9 setting Vcorrection to a second value equal to half
10 said Vagc first value;

11 performing the following first through fourth steps m
12 times in sequence:

13 a first step of measuring one or more in-phase and
14 quadrature digital samples;

15 a second step of converting of said samples into an rms
16 value;

17 a third step of comparing said rms value with a
18 threshold value and adding said Vcorrection to said Vagc if
19 said rms value is greater than said threshold value, and
20 subtracting said Vcorrection from said Vagc if said rms
21 value is less than said threshold value;

22 a fourth step of halving the value of said Vcorrection.

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24 11) The process of claim 10 where said m is one of the
25 values 3, 4, or 5.

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2 12) The process of claim 10 where said Vagc maximum
3 value is $2^{(n-1)}$.

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5 13) The process of claim 10 where said digital gain
6 correction value is $2^{(n-k-1)}$, and k is the number of the
7 iteration, starting at 1.

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9 14) The process of claim 10 where said digital
10 Vcorrection value is positive.

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12 15) The process of claim 10 where said digital
13 Vcorrection value is negative.

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15 16) the process of claim 10 where said first through
16 fourth steps comprise an iteration time having a first value
17 during a first interval, and said iteration time is longer
18 than said first value during a second interval following
19 said first interval.

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21 17) The process of claim 16 where said first interval
22 corresponds to the preamble time T1 of a wireless ethernet
23 packet.

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1 18) The process of claim 16 where said second interval
2 corresponds to the frame time T2 following the preamble time
3 T1 of a wireless ethernet packet.

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5 19) The process of claim 10 where said m times occurs
6 during a preamble time T1 of a wireless ethernet packet.

7
8 20) An RF front end comprising:
9 an RF receiver having a digital gain control input of
10 width n and producing a quadrature output digital value;
11 a digital gain controller producing an output Vagc
12 coupled to said digital gain control input in response to
13 said quadrature output digital values, said output Vagc
14 generated by:
15 setting Vagc to an initial value $2^{(n-1)}-1$ and setting an
16 iteration variable k to 0;
17 performing the following first through fourth steps
18 while said k is less than said m:
19 a first step of measuring said quadrature digital
20 values and producing the rms value of said quadrature
21 digital values;
22 a second step of comparing said rms value to a
23 threshold value;
24 a third step of adding a correction value $2^{(n-k-1)}$ to
25 said Vagc if said rms value is greater than said threshold,

1 and subtracting a correction value $2^{(n-k-1)}$ from said Vagc if
2 said rms value is less than said threshold;
3 a fourth step of incrementing said k.
4

5 21) The process of claim 20 where said m is one of the
6 values 3, 4, or 5.
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9 24) The process of claim 20 where said digital
10 correction value is positive.
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12 25) The process of claim 20 where said digital
13 correction value is negative.
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15 26) the process of claim 20 where said first through
16 fourth steps comprise an iteration time having a first value
17 during a first interval, and said iteration time is longer
18 than said first value during a second interval following
19 said first interval.
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21 27) The process of claim 26 where said first interval
22 corresponds to the preamble time T1 of a wireless ethernet
23 packet.
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1 28) The process of claim 26 where said second interval
2 corresponds to the frame time T2 following the preamble time
3 T1 of a wireless ethernet packet.

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5 29) The process of claim 20 where said m times occurs
6 during a preamble time T1 of a wireless ethernet packet.

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9 30) A digital gain control system for a multiplexed
10 stream of first and second quadrature stream of data
11 comprising two instances of the same process, each said
12 instance operating exclusively on either said first or said
13 second quadrature stream of data, said process comprising:
14 an rms voltage converter receiving one or more digital
15 inputs and forming an rms value;
16 a digital gain controller having:
17 an iteration variable set to an initial value;
18 a digital gain value having n bits, said digital gain
19 value having a maximum value and a minimum value, said
20 digital gain value being initially set to the median of said
21 maximum value and said minimum value;
22 a correction value having an initial value which is
23 half of said digital gain initial value;
24 an iteration process which performs the following
25 sequential steps m times:

1 comparing the value from said rms voltage converter to
2 a threshold voltage value;
3 adding said correction value if said rms voltage
4 converter is greater than said threshold voltage level, or
5 subtracting a correction value if said rms voltage converter
6 is less than said threshold voltage level;
7 halving said correction value.
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9 31) the process of claim 30 where said first through
10 fourth steps comprise an iteration time having a first value
11 during a first interval, and said iteration time is longer
12 than said first value during a second interval following
13 said first interval.
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15 32) The process of claim 30 where said first interval
16 corresponds to the preamble time T1 of a wireless ethernet
17 packet.
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19 33) The process of claim 30 where said second interval
20 corresponds to the frame time T2 following the preamble time
21 T1 of a wireless ethernet packet.
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23 34) The process of claim 30 where said m times occurs
24 during a preamble time T1 of a wireless ethernet packet.
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2 35) An RF front end comprising:
3 a first RF receiver having a digital gain control input
4 of width n and producing a first quadrature output digital
5 value including a first I value and a first Q value;
6 a second RF receiver having a digital gain control
7 input of width n and producing a second quadrature output
8 digital value including a second I value and a second Q
9 value;
10 a multiplexer converting said first I value and said
11 second I value into a stream of alternating first and second
12 I values, and also converting said first Q value and said
13 second Q value into a stream of alternating first and second
14 Q values;
15 a digital gain controller coupled to said stream of
16 alternating I values and said stream of alternating Q values
17 and producing a first output Vagc and a second output Vagc,
18 each said first Vagc and said second Vagc independently
19 generated by:
20 setting Vagc to an initial value $2^{(n-1)}-1$ and setting an
21 iteration variable k to 0;
22 performing the following steps while said k is less
23 than said m:

1 a first step of measuring said quadrature digital
2 values and producing the rms value of said quadrature
3 digital values;
4 a second step of comparing said rms value to a
5 threshold value;
6 a third step of adding a correction value $2^{(n-k-1)}$ to
7 said Vagc if said rms value is greater than said threshold,
8 and subtracting a correction value $2^{(n-k-1)}$ from said Vagc if
9 said rms value is less than said threshold;
10 a fourth step of incrementing said k.

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12 36) the process of claim 35 where said first through
13 fourth steps comprise an iteration time having a first value
14 during a first interval, and said iteration time is longer
15 than said first value during a second interval following
16 said first interval.

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18 37) The process of claim 36 where said first interval
19 corresponds to the preamble time T1 of a wireless ethernet
20 packet.

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22 38) The process of claim 36 where said second interval
23 corresponds to the frame time T2 following the preamble time
24 T1 of a wireless ethernet packet.

1 39) The process of claim 36 where said m times occurs
2 during a preamble time T1 of a wireless ethernet packet.

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5 40) A process for generating a first value Vagc and a
6 second value Vagc from an alternating stream of first
7 quadrature data and second quadrature data, where said first
8 Vagc is derived exclusively from said first quadrature data
9 and said second Vagc is derived exclusively from said second
10 quadrature data, where each said first Vagc and said second
11 Vagc are each digital values having n bits, said process
12 comprising for each said first and second Vagc:

13 setting Vagc to a first value;

14 setting Vcorrection to a second value equal to half

15 said Vagc first value;

16 performing the following steps m times in sequence:

17 measuring one or more in-phase and quadrature digital
18 samples;

19 converting of said samples into an rms value;

20 comparing said rms value with a threshold value and

21 adding said Vcorrection to said Vagc if said rms value
22 is greater than said threshold value, and subtracting said
23 Vcorrection from said Vagc if said rms value is less than
24 said threshold value;

25 halving the value of said Vcorrection.

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2 41) the process of claim 40 where said first through
3 fourth steps comprise an iteration time having a first value
4 during a first interval, and said iteration time is longer
5 than said first value during a second interval following
6 said first interval.

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8 42) The process of claim 40 where said first interval
9 corresponds to the preamble time T1 of a wireless ethernet
10 packet.

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12 43) The process of claim 40 where said second interval
13 corresponds to the frame time T2 following the preamble time
14 T1 of a wireless ethernet packet.

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16 44) The process of claim 40 where said m times occurs
17 during a preamble time T1 of a wireless ethernet packet.

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